**DL & CO Question Bank**

**3 Mark Questions**

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| 3 | 1 | Write the basic performance equation. |
| 3 | 1 | Define clock rate. |
| 3 | 1 | What are the basic functional units of a computer |
| 3 | 2 | What is addressing modes? |
| 3 | 2 | Give a brief description about any three addressing modes? |
| 3 | 2 | Define direct mode and register indirect mode with examples. |
| 3 | 2 | What is an Immediate addressing Mode? |
| 3 | 2 | Give short notes on: a) Word length b)address space |
| 3 | 2 | Discuss the different ways to arrange byte addresses across memory words. |
| 3 | 2 | List the two basic memory operations with proper examples. |
| 3 | 2 | Compare RTN and ALN |
| 3 | 3 | Discuss the principle behind the Booth’s algorithm? |
| 3 | 3 | State the principle of operation of a carry look-ahead adder |
| 3 | 3 | Write the Add/subtract rule for floating point numbers |
| 3 | 3 | What are the main features of Booth’s algorithm? |
| 3 | 3 | How floating point numbers can be represented in IEEE format? |
| 3 | 4 | Which are the three basic steps to execute an instruction? |
| 3 | 4 | What is the sequence of operations to add the contents of register R1 to those of R2 and store the result in R3? |
| 3 | 4 | Give the purpose of MFC signal? |
| 3 | 4 | Compare hardwired and micro programmed controls. |
| 3 | 4 | Write the register transfer sequence to read a word from memory. |
| 3 | 4 | What is hardwired control? How is it different from micro-programmed control? |
| 3 | 4 | What is control Word and control address registers? |
| 3 | 4 | Write down the control sequence for Move (R1), R2. |
| 3 | 4 | Discuss the different ways to organize microinstructions. |
| 3 | 4 | Briefly discuss bit-oring’ |
| 3 | 4 | What is the role of MAR and MDR? |
| 3 | 4 | What is microprogrammed control unit? |
| 3 | 5 | What is RISC? |
| 3 | 5 | What is CISC? |
| 4 | 1 | Illustrate the Memory Hierarchy. |
| 4 | 1 | Describe the purpose of MAR & MDR in Memory - Processor communication. |
| 4 | 1 | What are the different types of ROM? |
| 4 | 1 | Write a short note on Dynamic RAM . |
| 4 | 1 | Explain why Cache access is faster than Main memory access. |
| 4 | 1 | State Locality of Reference with reference to Cache memory. |
| 4 | 2 | Explain Virtual Memory. |
| 4 | 2 | Describe the benefits of using Virtual Memory. |
| 4 | 2 | Under what circumstances do page faults occur? |
| 4 | 2 | Briefly explain Secondary memory. |
| 4 | 2 | Differentiate Virtual Address and Physical address. |
| 4 | 2 | Define Hit Ratio. |
| 4 | 3 | What is Memory mapped I/O? |
| 4 | 3 | Illustrate I/O interface for an input device. |
| 4 | 3 | What is the purpose of SIN and SOUT bits? |
| 4 | 3 | Explain Program controlled I/O. |
| 4 | 3 | What are the different methods to access I/O devices? |
| 4 | 4 | What is interrupt? |
| 4 | 4 | Explain the function of Interrupt Service Routine. |
| 4 | 4 | Describe Vectored Interrupts. |
| 4 | 4 | How simultaneous interrupt requests from multiple devices are handled? |
| 4 | 4 | Mention any two uses of Interrupts in OS. |
| 4 | 5 | What is the purpose of Direct Memory Access? |
| 4 | 5 | Explain DMA transfer. |
| 4 | 5 | Describe the function of DMA controller. |
| 4 | 5 | For what types of operations is DMA useful? |
| 4 | 5 | Define Bus arbitration. |
| 4 | 5 | What are the different types of buses used in DMA? |
| 5 | 1 | Define parallel processing. |
| 5 | 1 | Define instruction stream and data stream. |
| 5 | 1 | What are parallel computer structures? |
| 5 | 1 | Explain vector processors? |
| 5 | 1 | What are SIMD array processors? |
| 5 | 2 | Define unified memory access, non-unified memory access in multiprocessor model. |
| 5 | 2 | Describe briefly the structure of multiprocessors. |
| 5 | 2 | What is time shared common bus structure? |
| 5 | 2 | Compare between shared and distributed memory |
| 5 | 2 | Explain any 2 interconnection networks. |
| 5 | 3 | What is meant by pipelining? |
| 5 | 3 | What are arithmetic pipelines? |
| 5 | 3 | Define instruction cycle phases. |
| 5 | 3 | Define structural hazards, data hazards in instruction pipelining. |
| 5 | 3 | What is meant by instruction pipelining? |
| 5 | 4 | Differentiate between superscalar and super pipelined systems. |
| 5 | 4 | Is there any difference between multicore and multiprocessor systems? |
| 5 | 4 | Define instruction level parallelism. |
| 5 | 4 | What are the advantages of multiprocessing. |
| 5 | 4 | Define multicore systems. |

**9Mark Questions**

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| 7 | 1 | (a)Draw and Explain single bus organization of datapath inside a processor  OR  (b)Explain the micro-programmed control unit in detail. |
| 8 | 1 | (a) Draw and explain the block diagram of a computer  OR (b) Explain Booth Algorithm with an example |
| 8 | 1 | (a) Explain different types of address formats with examples. Compare their relative merits and demerits.  OR (b) Explain IEEE floating point representation |
| 8 | 1 | (a) Explain how the expression ADD A B C will be executed in one address, two address and three  address processors in an accumulator organization.  OR  (b) Discuss in detail about the hardwired control unit with block diagram |
| 8 | 1 | (a)Draw and Explain single bus organization of datapath inside a processor OR (b)Explain the micro-programmed control unit in detail. |
| 8 | 1 | (a)Describe the significance of various addressing modes. OR (b)Compare and contrast RISC and CISC |
| 9 | 1 | A) Explain the various memory classifications.  OR B) Describe how interrupts are handled by the processor? |
| 9 | 1 | A) Explain Random Access Memory in detail.  OR B) Describe DMA and its operations. |
| 9 | 1 | A) Explain Cache memory and its advantages.  OR B) Explain various methods for accessing I/O devices. |
| 9 | 1 | A) Describe how cache memory is used to increase system performance  OR B) Explain Direct Memory Access in detail |
| 9 | 1 | A) Describe Memory Management requirements in detail.  OR B) Explain the working of Interrupts. |
| 10 | 1 | A) Explain the Flynn’s classification architecture of parallel processing.  OR B) Explain the interconnection structures used in multiprocessors. |
| 10 | 1 | a)Explain how memory organization can be done in multiprocessors.  OR b)Explain in detail the following SIMD parallel structures: Array Processors, Vector Processors |
| 10 | 1 | a)Explain instruction pipelining with its hazards  OR  b)Explain how arithmetic pipeline is used in floating point operations. |
| 10 | 1 | a)Explain the concepts: Instruction pipelining and Instruction level parallelism.  OR b)Explain in deail the advanced concepts: Superscalar systems, Super pipelined systems, Multicore systems |